

SAIT JABALPUR

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

EX - 403

DIGITAL ELECTRONICS LOGIC DESIGN LAB

LIST OF EXPERIMENT

1. TO TEST & STUDY THE OPERATION OF ALL LOGIC GATES USING VARIOUS IC'S.
2. IMPLEMENTATION OF AND, OR, NOT, NOR, EX-OR & EX-NOR GATES BY NAND & NOR UNIVERSAL GATES IC'S.
3. DESIGN & IMPLEMENTATION THE HALF ADDER & FULL ADDER CIRCUIT.
4. DESIGN & IMPLEMENTATION THE HALF SUBTRACTOR & FULL SUBTRACTOR CIRCUIT.
5. DESIGN & IMPLEMENTATION A BCD TO EXCESS-3 CODE CONVERTER USING NAND-NAND LOGIC.
6. TO TEST & STUDY THE RS, JK, T & D FLIP FLOP.
7. DESIGN & IMPLEMENTATION OF BOOLEAN FUNCTION USING MULTIPLEXER.
8. DESIGN & IMPLEMENTATION OF BOOLEAN FUNCTION USING DEMULTIPLEXER.
9. DESIGN & IMPLEMENTATION OF ANALOG TO DIGITAL CONVERTOR.
10. DESIGN & IMPLEMENT OF DIGITAL TO ANALOG CONVERTOR.

S.NO.	NAME OF EXPERIMENT	PAGE NO.	DATE	GRADE/TOTAL	REMARK	SIGN
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EXPERIMENT NO: 1

Objectives:-

To test & study the operation of all logic gates using various IC'S.

Apparatus Required:-

1. Trainer Kit Method: - Trainer Kit, Digital Multimeter, Patch Cords.
2. Bread Board Method :- Bread Board, +5V DC Power Supply, LED and Hookup Wires, Digital Multimeter.

Components Required:-

IC 7400 NAND, IC 7402 NOR, IC 7404 NOT, IC 7408 AND, IC 7432 OR, IC 7486 EX-OR.

Introduction:-

Now a day an automation system is based on digital electronics. The basic building blocks of digital electronics are its logic gates like AND, OR, NOT, NAND, NOR, X-OR. It is necessary to study the truth table of various gates behind this before proceeding for digital electronics. Logic gate trainer contains all the above gate ICs. Also basic logic gates can be formed-using BJT and diodes with built in regulated power supply, logic generator and logic output indicators, arranged in trainer form. To study the various results of different gates. First apply +5V and ground then connect inputs of the gates to logic generator (D0- D9) section and to observe the output connect its output terminals to logic indicator Q0-Q9 section.

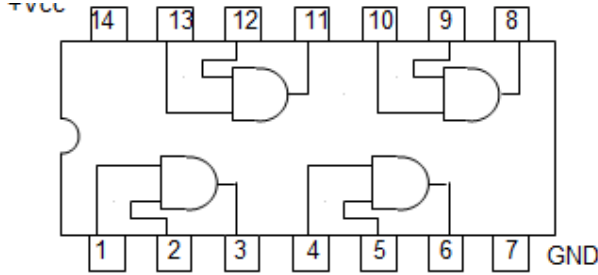
Theory: -

AND GATE

The AND gate is a logic circuit which has two or more inputs and a single output. AND gate provides product of Input signal at O/P. Hence for any AND gate output will be logic one, when all the inputs are high (logic 1). Fig (1) & Table 1 shows the symbol and truth table of AND gate. Fig (2) shows the internal block diagram of IC 7408(AND Gate).



Fig:-1



INPUT		OUTPUT
A	B	$Y=A.B$
0	0	0
0	1	0
1	0	0
1	1	1

Table:-1

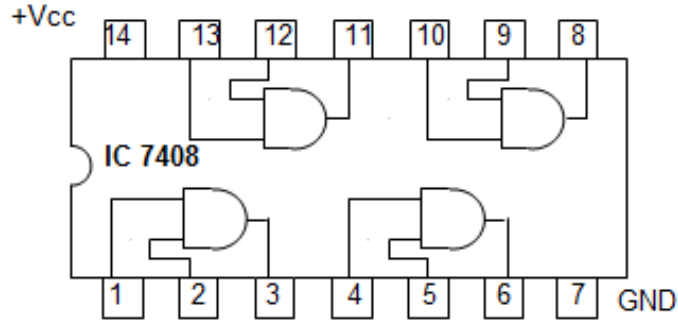


Fig:-2

Procedure:-

- 1) Study IC 7408 internal pins shown in fig 2.
- 2) Select any one gate (say 1).
- 3) For AND 1, input pins are 1 & 2, output pin is 3.
- 4) Apply logic inputs (1 or 0) from logic generator section using patch cords.
- 5) Connect output pin 3 to any one output Q0-Q9 of logic indicator section.
- 6) Vary inputs applied and verify the truth table as given in table 1.
- 7) Repeat above steps for other gate of IC 7408.

NAND GATE

The term NAND is a contraction of the expression NOT-AND. A NAND gate therefore, is an AND gate followed by an inverter. The output of a NAND gate is binary '0' if all its inputs are binary 1. Fig (3) & table 2, shows symbol, and truth table of NAND gate.

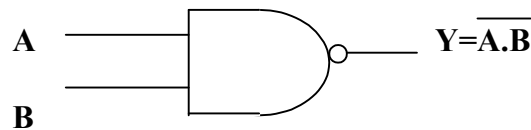


Fig:-3

Fig 3 & Table 2 shows the symbol and truth table of NAND gate. Fig 4 shows the internal block diagram of IC 7400(NAND Gate).

INPUT		OUTPUT
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Table:-2

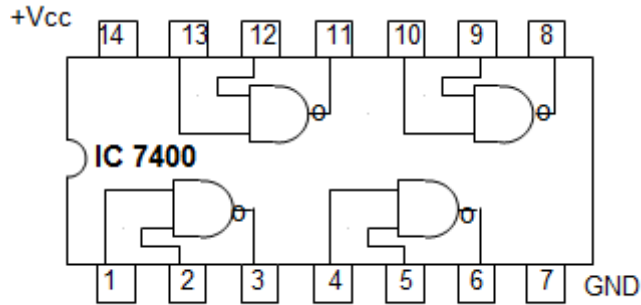


Fig:-4

Procedure :-

- 1) Study the internal pin diagram of IC 7400 as shown in fig 4.
- 2) Select any one NAND gate (say 1).
- 3) The inputs to NAND 1 are pin no. 1 & 2, while the output is pin no. 3.
- 4) Apply the logic inputs (1 or 0) from logic generator section using patch chords.
- 5) Connect output pin 3 to any one output of Q0 or Q1 of the logic indicator section.
- 6) Change input applied and verifies the truth table as given in table 2.
- 7) Repeat the above steps for another NAND gate.

OR GATE

Voltage is high (logic 1) if any or all of the I/P are high (logic 1) and the o/p becomes low (logic 0) only when all the I/P are low (logic 0).



Fig:-5

Fig 5 & Table 3 shows the symbol and truth table of OR gate. Fig 6 shows the internal block diagram of IC 7432(OR Gate).

INPUT		OUTPUT
A	B	$Y=A+B$
0	0	0
0	1	1
1	0	1
1	1	1

Table:-3

Procedure 3:-

- 1) Study the internal pin configuration of IC 7432 as shown in fig 6.
- 2) Select any one OR gate (say 1).
- 3) For first OR gate the input pins are 1 & 2 and the output pin is 3.
- 4) Apply the logic input (1 or 0) from logic generator.
- 5) Connect output pin 3 to any one output of Q0 or Q1 of the logic indicator section.
- 6) Change the input applied and verifies the truth table ass given in table 3.
- 7) Repeat the above steps for another OR gates.

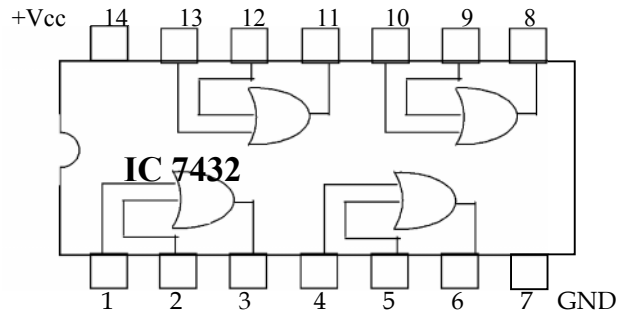


Fig:-6

NOR GATE

NOR gate can be constructed by giving the o/p of OR gate to NOT gate. In NOR Gate all the I/Ps must be low (logic 0) to get a high o/p (logic 1) and the o/p is low (logic 0) if any I/P is high (logic 1).



Fig:-7

Table:-4

INPUT		OUTPUT
A	B	$Y=\overline{A+B}$
0	0	0
0	1	1
1	0	1
1	1	1

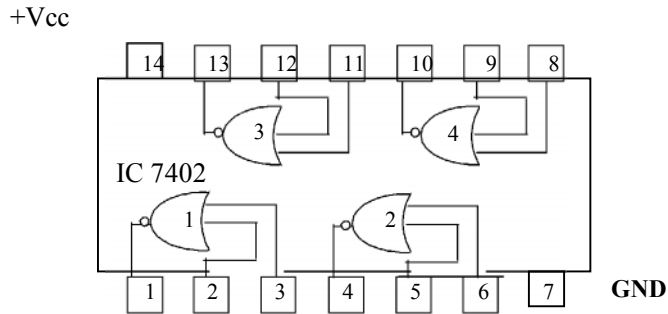


Fig 8

The integrated circuit 7402 contains four identical NOR gates with totem-pole outputs.

Procedure 4:

- 1) Study the internal pin configuration of IC 7402 as shown in fig 8.
- 2) Select any one NOR gate (say 1).
- 3) For first NOR gate the input pins are 2 & 3 and the output pin is 1.
- 4) Apply the logic input (1 or 0) from logic generator.
- 5) Connect output pin 1 to any one output of Q0 or Q1 of the logic indicator section.
- 6) Change the input applied and verifies the truth table as given in table 4.
- 7) Repeat the above steps for another NOR gates.

EX-OR GATE

The exclusive OR gate is sometimes referred to as the “any but not all gate”. The term “exclusive OR gate “is often shortened to “XOR gate”. OR gate shown in fig 9 and truth table is shown in table 5.

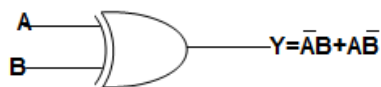
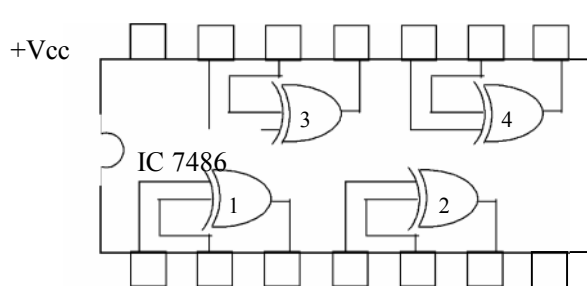


Fig:-9



INPUT		OUTPUT
A	B	$Y = \overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

Fig 10

Table:-5

IC-7486 consists of 4 dual I/P X-OR gate. In two I/P (X-OR) gate the necessary condition for O/P Y to be equal to 1 is that any one of the two I/P's should be 1 else for all other conditions O/P Y=0. The logical equation of EX-OR gate is $\overline{A}B + A\overline{B}$. In EX-OR gate when both the I/P's are equal then output y=0. If both the I/P are unequal then o/p of EX- OR gate y=1

Procedure 5:

- 1) Study the internal pin configuration of IC 7486 as shown in fig 10.
- 2) Select any one EX-OR gate (say 1).
- 3) For first EX-OR gate the input pins are 1 & 2 and the output pin is 3.
- 4) Apply the logic input (1 or 0) from logic generator.
- 5) Connect output pin 3 to any one output of Q0 or Q1 of the logic indicator section.
- 6) Change the input applied and verifies the truth table as given in table 5.
- 7) Repeat the above steps for another EX-OR gates.

6) NOT GATE

A NOT gate is a gate with only one I/p and one o/p. It is also called an inverter because the o/p is always opposite to the I/P i.e. when the I/P voltage is high (logic 1), the o/p is low (logic 0). On the other hand when the I/P voltage is low (logic 0) the o/p is high, (logic 1). The relation between I/p state & o/p state of a NOT gate are shown in following truth table. Fig shows the symbol of NOT gate.



Fig:-11

+ Vcc

INPUT	OUTPUT
A	$\overline{Y=A}$
0	1
1	0

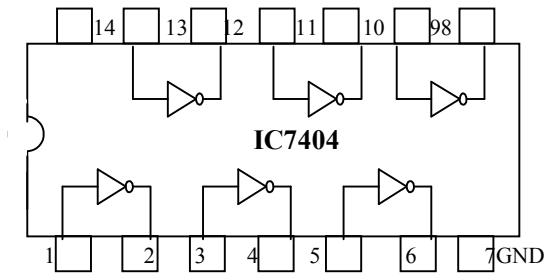


Table:-6

Fig:-12

Procedure 6:

- 1) Study the internal pin configuration of IC 7404 as shown in fig 14.
- 2) Select any one NOT gates (say 1).
- 3) For first NOT gate the input pins are 1 & 2 is the output pin.
- 4) Apply the logic input (1 or 0) from logic generator section to the input of the gate.
- 5) Connect output pin 2 to any one output of Q1 or Q1 of the logic indicator section.
- 6) Change the input applied and verifies the truth table as given in table 7.
- 7) Repeat the above steps for another NOT gates.

Using Bread Board-

- 1) Connect the circuit as per circuit diagram.
- 2) Connect the input terminal to the Input pins of IC.
- 3) Connect the Output terminal to the Logic Indicator.
- 4) Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC.
- 5) Verify the truth table.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

- Q.1 What do you mean by Logic Gates?
- Q.2 What are the applications of Logic Gates?
- Q.3 What is Truth Table?
- Q.4 Why we use basic logic gates?
- Q.5 Write down the truth table of all logic gates?

EXPERIMENT NO: 2

Objective:

To verify the Truth Table of EX-OR and EX-NOR gate using Universal Gate.

Apparatus Required:-

Bread Board,+5V DC Power Supply, LED and Hookup Wires, Digital Multimeter.

Components Required:-

NAND Gate IC-7400, NOR Gate IC-7402.

Theory:

UNIVERSAL GATE: - NAND and NOR Gate are called Universal gates because both can be used to implement any gate like AND, OR, NOT, EX-OR and EX-NOR Gate or any combination of these basic gates.

NAND GATE: - NAND Gate is a contraction of the AND-NOT gates. It has two or more inputs and only one output. When all inputs are high the output is low. If any one or both the inputs are low, then the output is high. The small circle or bubble represents the operation of inversion.

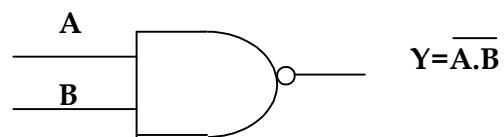
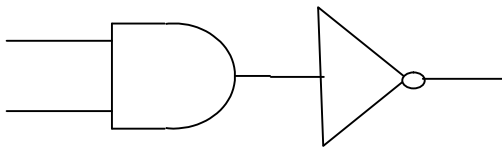
OUTPUT IS: - $Y = \overline{A.B}$

TRUTH TABLE:-

Input		Output
A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

$Y = A.B$

Table



NOR GATE: - NOR Gate is a contraction of the NOT-OR gates. It has two or more inputs and only one output. The output is high only when all the inputs

are low. If any one or both input is high, and then the output is low. The small circle or bubble represents the operation of inversion.

OUTPUT IS: - $Y = \overline{A+B}$

TRUTH TABLE:-

Input		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE OF EX-OR GATE

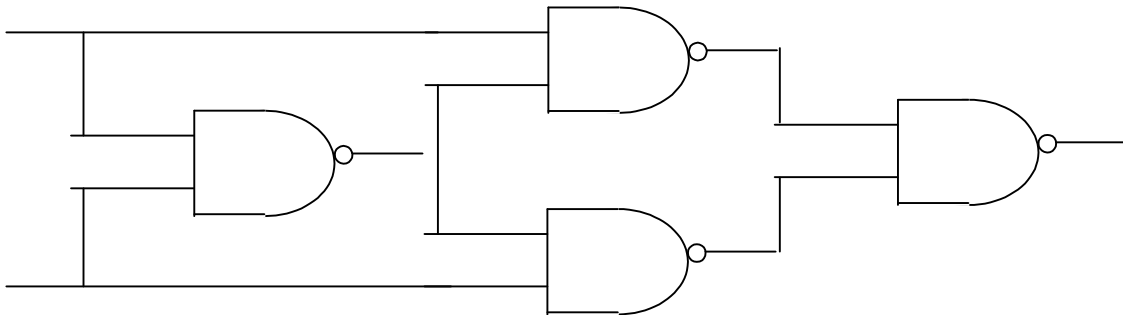
Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE OF EX-NOR GATE

IMPLEMENTATION OF EX-OR AND EX-NOR GATE USING UNIVERSAL GATE

CIRCUIT DIAGRAM:-

A



B

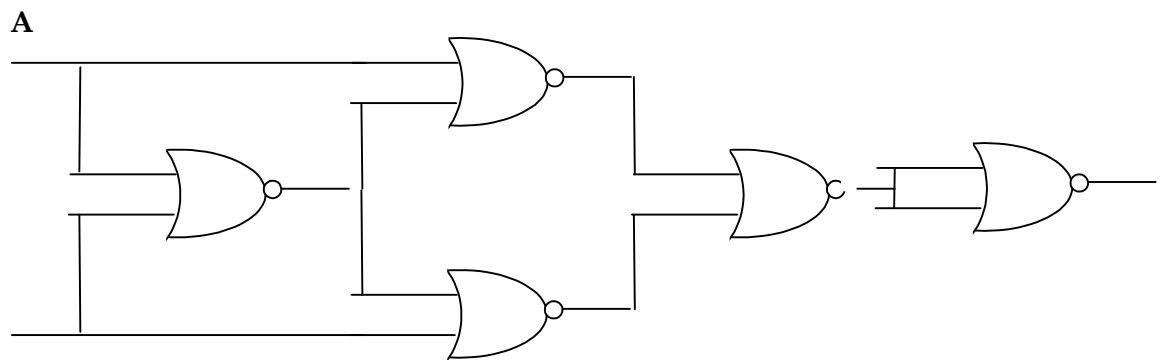
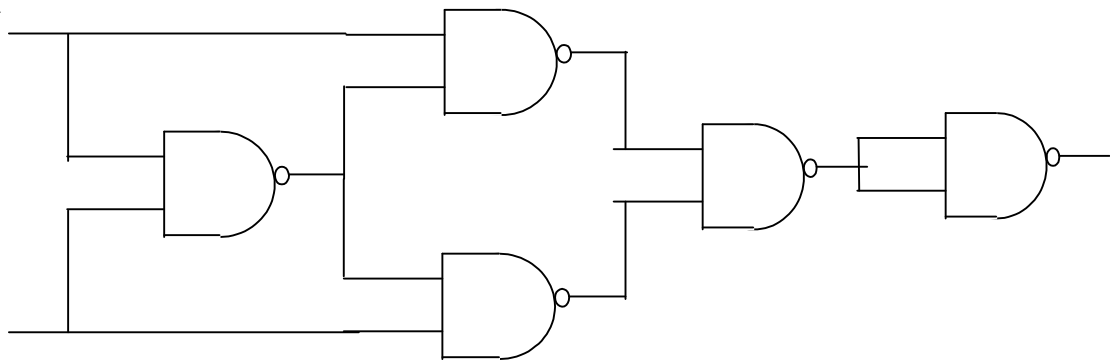


Fig: - Realization of EX-OR Gate Using NAND and NOR Gate

CIRCUIT DIAGRAM:-

A



B

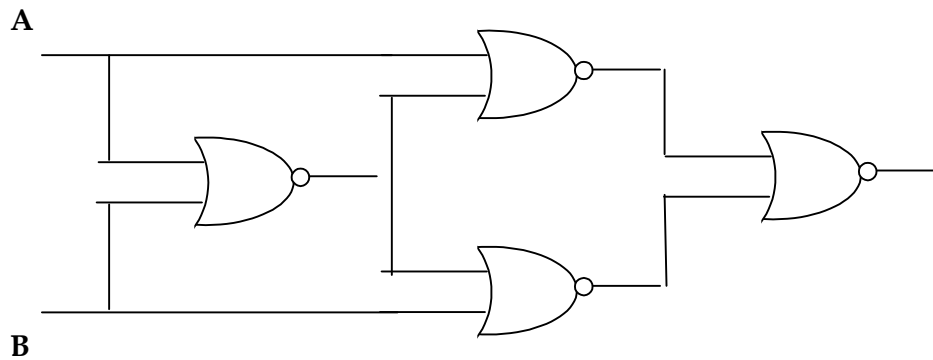


Fig: - Realization of EX-NOR Gate Using NAND and NOR Gate

PROCEDURE:-

Using Bread Board-

1. Connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 7 is connect the Ground and Pin no. 14 is connect the +5VCC.
5. Verify the truth table.

RESULT:-

Thus, we have verified the truth -table of EX-OR and EX-NOR gate using universal gates.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

- Q.1 What do you mean by universal gate?
- Q.2 Write truth table for 2 I/P OR, NOR, AND and NAND gate?
- Q.3 Implement all logic gate by using Universal gate?
- Q.4. Why is they called Universal Gates?
- Q.5 Give the name of universal gate?

EXPERIMENT NO: 3

Objectives:

Design & implementation the Half Adder and Full Adder.

Apparatus Required:

1. Trainer Kit Method:- Trainer Kit
2. Bread Board Method :- Bread Board,
+5V DC Power Supply,
LED and Hookup Wires,
Digital Multimeter.

Components Required:

IC 7486, IC 7408, IC 7432.

Theory:

By combining logic gate in the right way, circuits that can add can be formed binary bits. In binary system, any number can be represented with the combination of only two digits 0 and 1 as shown in binary addition table.

$$0 + 0 = 0$$

$$1 + 0 = 1$$

$$0 + 1 = 1$$

$$1 + 1 = 0, \text{ carry} = 1$$

For Half Adder:

Fig shows, a block symbol of half adder.

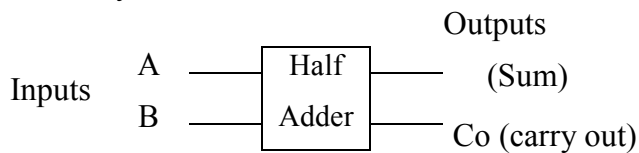


Fig:-1 Block Diagram of half adder

Truth table:

Inputs		Output	
A	B	Sum	Co
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

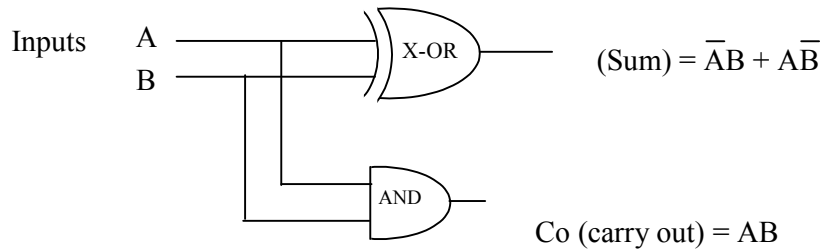


Fig:-2 Logic diagram of Half adder

Operation:

The output of the X-OR gate is called the () sum O/P while the O/P of the AND gate is the Carry (C0).

The AND gate produce a high O/P only when both I/P's are high [logic 1]. The X-OR gate produces a high O/P if, either of I/P is high.

(1) If A & B = 0

$$\begin{aligned}\text{Output Sum} &= \bar{A}.B + A.\bar{B} \\ &= \bar{0}.0 + 0.\bar{0} = 1.0 + 0.1 = 0 + 0 = 0\end{aligned}$$

$$\begin{aligned}\text{Output carry} &= A.B \\ \text{Co} &= 0.0 = 0\end{aligned}$$

Hence If A=0 & B=0 then Sum=0 & Co=0

(2) If A=0, B=1

$$\begin{aligned}\text{Output Sum} &= \bar{A}.B + A.\bar{B} \\ &= \bar{0}.1 + 0.\bar{1} = 1.1 + 0.0 = 1 + 0 = 1\end{aligned}$$

$$\text{Output carry} = A.B = 0.1 = 0$$

Hence If A=0 & B=1, then sum = 1 & carry =0.

(3) Similarly if $A=1, B=0$ then

Output sum =1 output carry =0

(4) If $A \& B =1$ then

Output sum = 0 & Output carry =1 (to next MSB)

For Full adder:

Half adder circuit is used to add two bits at a time. Full adder circuit is used for addition of three I/P at a time giving sum and carry out.

Following fig. 1 & 2 shows the Block schematic and logical diagram of Full Adder.

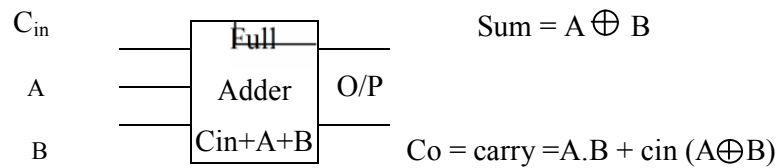


Fig :-1 Block Diagram of Full Adder

Truth Table:

Inputs			Output	
C_{in}	B	A	Sum	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

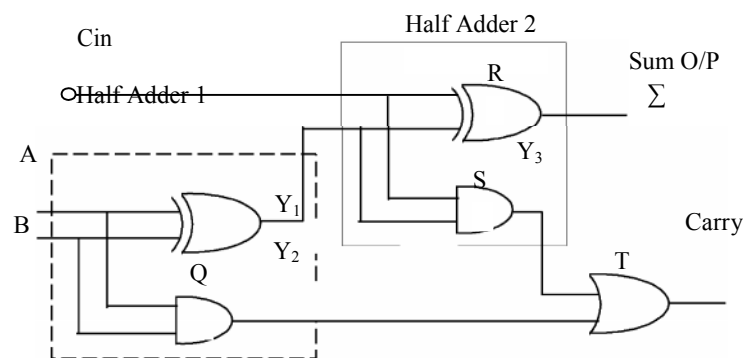


Fig:-2 Logical diagram for Full adder

Operation:

Consider any case of input combination. E.g. $C_{in} = 1, B=0, A=1$. Now refer fig (2).

Output of P gate, $Y_1 = \bar{A}.B + A.\bar{B} = 1.1 + 0.0 = 1$

Output of Q gate, $Y_2 = A.B$

$$= 1.0 = 0$$

Output of S gate, $Y_3 = C_{in}. Y_1$

$$= 1.1 = 1$$

$$\text{Sum} = C_{in}. \bar{Y}_1 + \bar{Y}_1.C_{in}$$

$$= 1.0 + 0.1 = 0 + 0 = 0$$

Carry out $C_o = Y_3 + Y_2$

$$= 1 + 0 = 1$$

Hence for $c_{in} = 1, B=0$ & $A=1$, then

Sum O/P = 0 and carry O/P = 1

Draw the Circuit Diagram for Bread Board Method

PROCEDURE:-

In Half and Full adder Trainer Kit-

1. Study the circuit given on front panel of kit
2. Switch ON the power supply & note that Red LED glows.
3. Measure & note the voltage for logic 1 & logic 0.

For Half Adder

1. Apply the I/P logic Combination (either 0 or 1) to A, B I/P's.
2. Connect the O/P C1 and S1 to O/P Logic indicators.
3. Verify and note down the Truth Table of Half Adder.

For Full Adder

1. Apply I/P logic Combination (either 0 or 1) to A, B & C I/P's.
2. Connect the C1 - C1 and S1 - S1 using Patch Chords.
3. Connect the O/P C0 and S0 to O/P Logic indicator
4. Verify and note down the Truth Table of Full Adder.

Using Bread Board-

1. Connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC.
5. Verify the truth table.

Observation for Half Adder:

Inputs		Output	
A	B	Sum	Carry
	0		
	1		

Observation table for Full Adder:

Inputs			Output	
C _{in}	A	B	Sum	Carry Co
0	0	0		
-	-	-		
-	-	-		

Result:

Half Adder Circuit adds the two bits and Full Adder Circuit adds the 3 Bit.
The Truth Table for the half & full adder is verified.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

- Q.1 Draw circuit diagram of Half Adder circuit?
- Q.2 Draw circuit diagram of Full Adder circuit?
- Q.3 Draw Full Adder circuit by using Half Adder circuit and minimum no. of logic gate?
- Q.4 Write Boolean function for half adder? Q.5 Write Boolean function for Full adder?
- Q.5 Design the half Adder & Full Adder using NAND-NAND Logic.

EXPERIMENT NO-: 4

Objectives:

Design & implementation the Half Subtractor and Full Subtractor.

Apparatus Required:

1. Trainer Kit Method: - Trainer Kit, Multimeter, Patch Chords.
2. Bread Board Method: - Bread Board,
+5V DC Power Supply,
LED and Hookup Wires,
Digital Multimeter.

Components Required:

IC 7486, IC 7408, IC 7432, IC 7404.

Theory:

By combining logic gate in the right way we can built circuits that can add and subtract binary bits. In binary system, any number can be represented with the combination of only two digits 0 and 1 as shown in binary subtraction.

$$0 - 0 = 0$$

$$1 - 0 = 1$$

$$1 - 1 = 0$$

$$0 - 1 = 1, \text{ borrow} = 1$$

For Half Subtractor:

Truth table:

Inputs		Output	
A	B	Diff	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Fig shows, a block symbol of half subtractor.

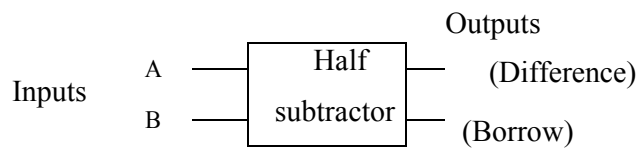
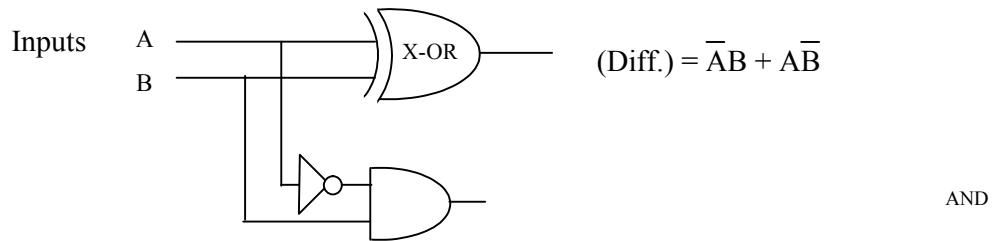


Fig :-1 Block symbol of half subtractor



$$\text{Borrow} = \bar{A}B$$

Fig:-2 Logic diagram of Half subtractor

Operation:

The output of the X-OR gate is called the difference (D) O/P while the O/P of the AND gate and NOT gate is the borrow (B0).

The AND gate produce a high O/P only when both I/P's are high [logic 1]. The X-OR gate produces a high O/P if, either of I/P is high.

(1) If A & B = 0

$$\begin{aligned} \text{Output difference} &= \bar{A}.B + A.\bar{B} \\ &= \bar{0}.0 + 0.\bar{0} = 1.0 + 0.1 = 0 + 0 \end{aligned}$$

$$\text{Difference} = 0$$

$$\begin{aligned} \text{Output borrow} &= \bar{A}.B \\ B_0 &= 1.0 = 0 \end{aligned}$$

Hence If A=0 & B=1, then diff. = 0 & borrow = 0.

For Full Subtractor:

A Full Subtractor circuit performs multibit subtraction where a borrow from the previous bit position may be included. A Full Subtractor has three inputs A (minuend), B (subtrahend), B_{in} (borrow in).

Following fig. 1 & 2 shows the Block schematic and logical diagram of Full Subtractor.

Truth Table:

Inputs			Output	
A	B	Bin	D	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

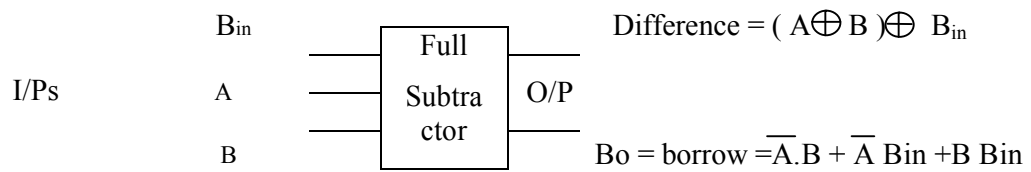


Fig (1) Block diagram of full subtractor

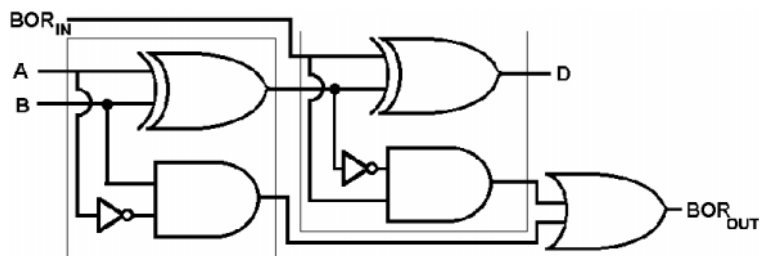


Fig (2) Logical diagram for full Subtractor

Operation

Consider any case of input combination. e.g. $A = 1, B=0, B_{in}=1$. Now refer fig (2).

(1) If $A = 0, B = 0$ & $B_{in}=1$

$$\begin{aligned}\text{Output Difference} &= A \oplus B \oplus B_{in} \\ &= A'B'B_{in} + A'BB'_{in} + AB'B'_{in} + ABB_{in} = 1\end{aligned}$$

$$\begin{aligned}\text{Output Borrow} &= A'B + A'B_{in} + BB_{in} \\ &= 1\end{aligned}$$

(2) If $A = 0, B = 1$ & $B_{in}=1$

$$\text{Output Diff.} = 0 \quad \text{Output Borrow} = 1$$

(3) If $A = 1, B = 0$ & $B_{in}=0$

$$\text{Output Diff.} = 1 \quad \text{Output Borrow} = 0$$

(4) If $A = 1, B = 1$ & $B_{in}=0$

$$\text{Output Diff.} = 0 \quad \text{Output Borrow} = 0$$

PROCEDURE:-

Using Bread Board-

1. Connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC.
5. Verify the truth table.

Observation for Half Subtractor:

Inputs		Output	
A	B	Diff.	Borrow

Observation table for Full Subtractor:

Input			Output	
A	B	B _{in}	Diff.	Borrow

Result:

Half Subtractor Circuit subtracts the two bits and Full Subtractor Circuit adds the 3 Bit. The Truth Table for the half & full Subtractor is verified.

VIVA QUESTIONS

- Q.1 Draw circuit diagram of Half Subtractor circuit?
- Q.2 Draw circuit diagram of Full Subtractor circuit?
- Q.3 Draw Full Subtractor circuit by using Half Subtractor circuit and minimum no. of logic gate?
- Q.4 Write Boolean function for half Subtractor?
- Q.5 Write Boolean function for Full Subtractor?

Draw the Circuit Diagram for Bread Board Method

EXPERIMENT NO.5

Objectives:

Design & implement A BCD to Excess-3 code converter.

Apparatus Required:

1. Trainer Kit Method: - Trainer Kit, Digital Multimeter, Patch Cords.
2. Bread Board Method: -Bread Board,
+5V DC Power Supply,
LED and Hookup Wires,
Digital Multimeter.

Components Required:

IC 7404; IC 7408; IC7486;

Theory:

There are many type of converter in the digital electronics. For ex. Grey to BCD & vice versa, Hexadecimal to Decimal converter and so on. One other type is to convert any decimal number into its excess-3. The Excess-3 number is obtained by adding 3 to the BCD no. If a BCD no. is 1 then its Excess-3 equivalent to

$$\begin{array}{r} + 1 \\ 3 \\ \hline 4 \end{array}$$

i.e. 0001+0011 = 0100.

Another example to convert 45 of decimal to excess-3 is

$$\begin{array}{r} + 4 \\ 3 \\ \hline 7 \\ \downarrow \\ 0111 \end{array} \quad \begin{array}{r} + 5 \\ 3 \\ \hline 8 \\ \downarrow \\ 1000 \end{array} \quad \begin{array}{l} \text{i.e. } 0100 + 0011 = 0111 \\ 0101 + 0011 = 1000 \end{array}$$

So, 01111000 is the Excess-3 code of 45 (01000101) BCD no.

Excess-3 code is an unweighted code; its code assignment is obtained from the corresponding value of BCD after the addition of 3. Each code uses four bits to represent a decimal digit, there must be four input variables and four output variables. Let us designate the four input binary variables by the symbol A,B,C and D, and the four output variables by W,X,Y and Z. The Truth Table relating the inputs and output variables is shown in given Table no.1.

Truth Table

Decimal Number	BCD number				Excess-3 number			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Procedure:

For Trainer Kit:

- 1) Study the circuit provided on the front panel of the kit.
- 2) Switch 'ON' the power supply.
- 3) Check the high low state of A to D using digital multimeter.
- 4) Select any BCD input A-D and observe Excess-3 output X-Z.
- 5) Verify truth table.

Using Bread Board-

1. Draw the circuit diagram and Connect the circuit.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC.
5. Verify the truth table.

Result: The BCD to Excess- 3 code conversion is studied and the truth table is verified.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

Q.1 What is Excess-3 code? Why it is called Excess-3 code?

Q.2 What is the application of Excess-3 Code?

Q.3 What is ASCII code?

Q.4 Excess-3 code is Weighted or Unweighted?

Q.5 Out of the possible 16 code combination? How many numbers used in Excess-3 code?

EXPERIMENT NO.6

Objectives:

To Test & Study the R-S & Clocked R-S, JK, and D Flip-Flop.

Apparatus Required:

1. Trainer Kit Method: - Trainer Kit, Multimeter, Patch Chords.
2. Bread Board Method: - Bread Board,
+5V DC Power Supply,
LED and Hookup Wires,
Digital Multimeter.

Components Required:

IC 7400 NAND gate IC, IC 7402 NOR gate IC, IC 7404 NOT gate IC.

Theory:

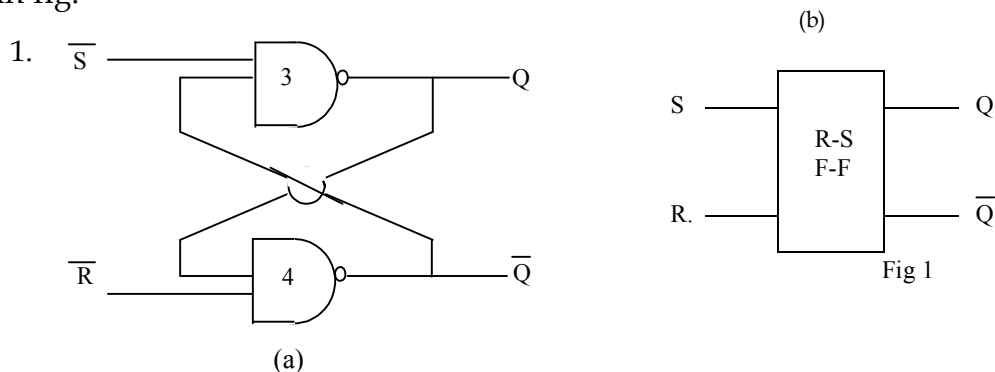
A flip-flop is a bistable electronic circuit that has two stable states i.e. its output is either 0 or +5Vdc. One of the easiest methods to construct a flip-flop is to connect two inverters in series. But basic flip-flop can be improved by replacing two inverters with either NAND or NOR gate. The additional input of these gates provides a conventional means for application of input signals to switch the flip-flop from one stable state to another. Two input NAND gate are connected to form a flip-flop circuit. These two inputs are R & S

The flip-flop has two outputs terms as Q and \bar{Q} . If flip-flop is put into one state it will remain in that state as long as power is applied or until it is changed. In digital circuits, flip-flops are used in variety of storage, counting, sequencing and timing applications.

R- S & CLOCKED R- S FLIP-FLOP

The R-S flip-flop is the simplest. It has two inputs, S & R and two outputs \bar{Q} & Q. applying appropriate logic signal to either S or R input, it will put the latch into one state or the other. When a flip-flop is set by S input, it is said to be storing binary 1. (Q O/P = high). When reset by R input, it is said to be storing binary 0 (Q O/P = low).

An R-S flip-flop constructed by cross-coupling two NAND gates as shown in fig:



Input		Output	
R	S	Q	\bar{Q}
0	0		Forbidden state
0	1	1	0
1	0	0	1
1	1	No Change	

Truth Table1

Fig 1 (b) shows the symbol of the R-S flip-flop. When both R-S input is binary 0, both Q & \bar{Q} output goes high. This condition is not allowed in normal use of flip-flops, as the \bar{Q} represents the complement output of Q. The truth table for RS flip-flop is given in table 1.

Procedure:

- 1) Study the circuit provided on the front panel of the kit.
- 2) Switch 'ON' the power supply.
- 3) Connect the Circuit as shown in Fig (1) i.e. S-R Flip Flop without clock, by using patch chords.
- 4) Connect Q to the output indicator circuit.
- 5) Apply the corresponding inputs and verify the truth table (1).
- 6) If necessary measure the output voltages.

Result:

Thus R-S Flip -Flop without clock is studied & Truth table is verified.

CLOCKED R-S FLIP- FLOP

A clocked R-S flip-flop can also be constructed by simply adding two NAND gates to the fig 1 as shown in fig 2.

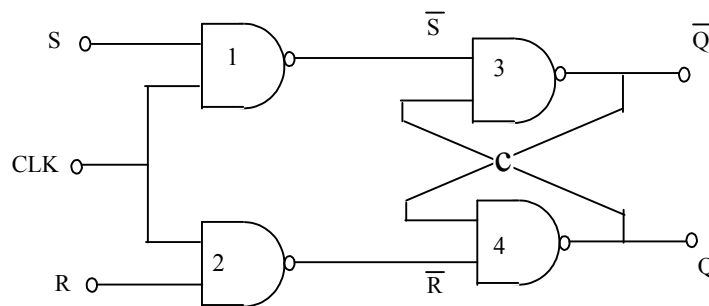


Fig 2

The truth table for R-S flip-flop is given in table 2.

CLK	Input		Output
	S	R	Q
1	0	0	No Change
1	0	1	0
1	1	0	1
1	1	1	Forbidden State

Truth Table 2.

Procedure:

- 1) Study the circuit provided on the front panel of the kit.
- 2) Switch 'ON' the power supply.
- 3) Now Connect the circuit as shown in fig (2) i.e. S-R Flip - Flop with clock by using patch chords.
- 4) Apply the corresponding inputs to S & R and apply the clock pulse.
- 5) Connect Q to the output indicator circuit.
- 6) Verify the truth table (2).
- 7) If necessary measure O/P voltages.

Result:

Thus R-S Flip -Flop with clock is studied and Truth table is verified.

D & CLOCKED D FLIP- FLOP

D FLIP- FLOP WITHOUT CLOCK

The R -S Flip Flop has two data inputs R & S. Generation of two signals to drive a flip-flop is a disadvantage in much application. Furthermore, the forbidden condition of both R and S high may occur inadvertently. This has led to the D Flip Flop a circuit that needs only a single data input.

Fig :-3 shows the simple diagram of D Flip- Flop using NOR Gate.

I/P	O/P
D	Q
0	0
1	1

Table 3.

Procedure:

- 1) Study the circuit provided on the front panel of the kit.
- 2) By using patch chord short the points 1& 2 and connect output Q to output indicators circuit.
- 3) Switch ON the supply.
- 4) Now by giving proper I/P , verify the truth table 3.

Result:

Thus D Flip- Flop without clock is studied and Truth table is verified.

CLOCKED D FLIP- FLOP

Fig (4).shows the simple way to build a delay D Flip- Flop .This kind of

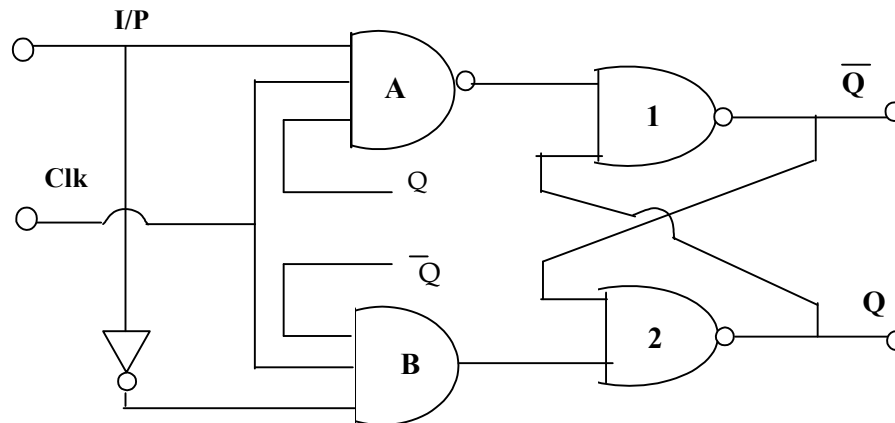


Fig 4.D Flip- Flop with Clock

Flip-Flop prevents value of D from reaching the Q output until a clock pulse occurs.

Truth Table 4.

Clk	D	Q_{n+1}
0	X	Q_n (last state)
1	0	0
1	1	1

As shown in the truth table 4, while the clock (Clk) is low, D is don't care, Q will remain latched in its last state. When the clock is high, Q takes on the last value of D. If D is changing while the clock is high, it is the last value of D that is stored.

Procedure:

- 1) Study the circuit provided on the front panel of the kit.

- 2) Apply the corresponding inputs to D and apply the clock pulse.
- 3) Connect Q to output indicator circuit.
- 4) Observe output and verify its truth table 4.
- 5) If necessary measure the output voltages.

Result:

Thus Clocked D Flip -Flop is studied and truth table is verified.

3 JK FLIP-FLOP

The J-K Flip-flop is the most versatile binary storage element. It can perform all the functions of RS and D flip-flop JK flip-flop two flip-flop in one. These are called master and slave flip-flop. The o/p of second flip-flop will directly copy the o/p of first flip-flop. Hence the first flip-flop is called master and 2nd flip-flop is called slave flip-flop.

Fig (5) shows the symbol of JK flip-flop & table (5) shows the truth table.

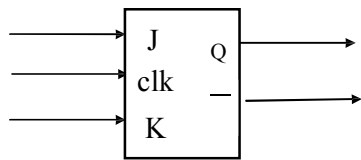


Fig. (5)

Input		Output
J	K	Q
0	0	Q _n
0	1	0
1	0	1
1	1	Q _n

Truth Table 5.

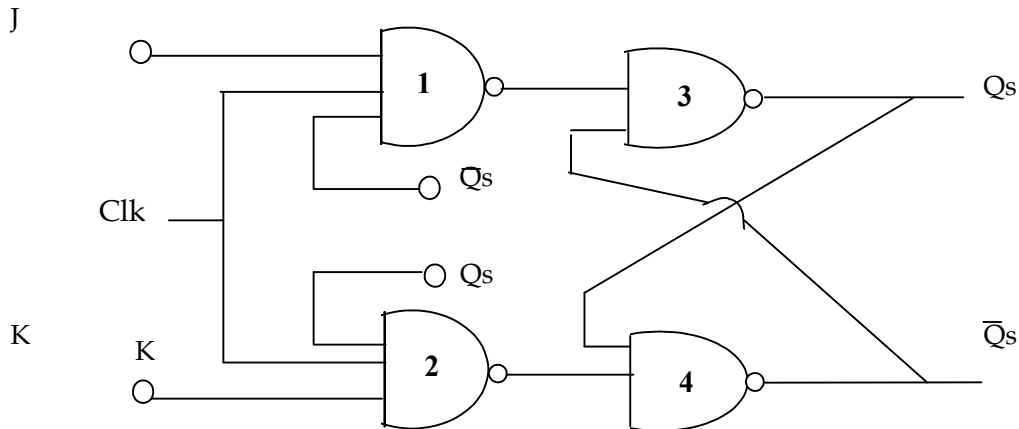


Fig:- JK Flip Flop

Procedure:

- (1) Study the circuit given on the front panel of the kit.
- (2) Switch 'ON' the power supply.
- (3) Apply proper I/P to the J &K using patch chord. Note O/P levels when the clock pulse input line goes high (logic 1) and when it goes low (logic 0).
- (4) If J & K = 0 (logic 0) the O/P of the Q is Qn. So the operation of F/F is inhabited.
- (5) When I/P J=0 (logic 0) and K=1 (logic 1) then the O/P of Q (Reset).
- (6) When the I/P J = 1 (logic 1) and K = 1 (logic 1) then the F/F toggles on every clock pulse.
- (7) See the o/p of F/F and verify the truth table

Observation table:

Input			Output
Clock	J	K	Q
	0	0	-
	0	1	-
	1	0	-
	1	1	-

Result:

Thus JK Flip -Flop is studied and truth table is verified.

Using Bread Board-

1. Connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC.
5. Verify the truth table.

Result:

Thus R-S Flip -Flop, D Flip- Flop, Clocked D Flip -Flop, JK Flip -Flop, is studied and truth table is verified.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

Q.1 What is Flip-Flop?

Q.2 What is Latch circuit?

Q.3 Draw a truth -tables of S-R, J-K, D and T?

Q.4 What is the disadvantages of S-R Flip-Flop?

Q.5 How can you remove the problem of S-R Flip -Flop?

Q.6 Make circuit diagram of S-R, J-K, D and T Flip-Flop?

Q.7 What do you understand by Race Aground condition? How it is over come in J-K Flip Flop?

EXPERIMENT NO:7

Objective:

To Study 4:1 Multiplexer Using Various IC's.

AppratusRequired:

1. Trainer Kit Method: - Trainer Kit,Digital Multimeter,Patch Cords.
2. Bread Board Method: - Bread Board,+5V DC Power Supply,LED and Hookup Wires,Digital Multimeter.

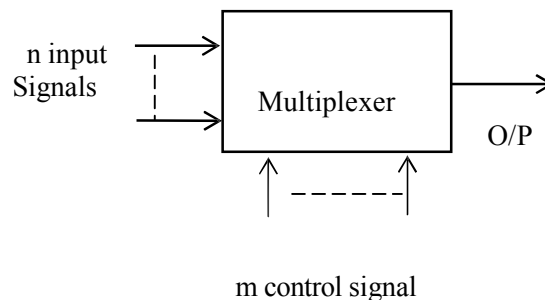
Components Required:

IC- 74153, IC- 7432, IC-7408,IC-7404.

Theory:

Multiplex means many into one. A multiplexer is a Circuit with many I/Ps but only one O/P. By Applying Control Signal, we can Steer any I/P to the O/P.

Following fig Shows the block Diagram of the Multiplexer. The Multiplexer has n I/P Signals, m Control Signals and 1 O/P Signal



4 to 1 Multiplexer:

4 to 1 MUX using IC 74153 has been shown on the Front Panel of the Kit. In this there are Two Control Signals 4 I/P Signals and One O/P Signal. Control Signal is applied to A1 A0 & I/P is given to D0 to D3 pins and O/P Q is taken from O/P pin.

Depending upon the control Signal the Data at I/P is Produced at the O/P. for eg. If the I/P to A1 A0 is 01 then the Data at D1 pin is Transmitted at O/P.

Following fig shows the Pin Configuration & Truth Table of IC 74153

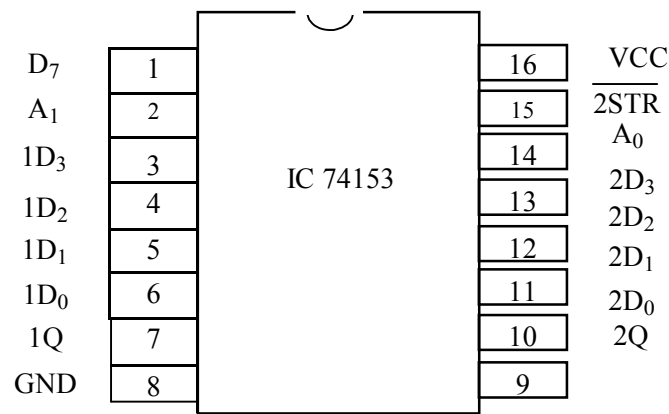


Fig 2: Pin out diagram of IC 74153

I/P			O/P
STR	A1	B1	Q
1	X	X	0
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3

Procedure:

1. Switch ON the Power Supply.
2. Measure the Voltage at Pin no 16 using DMM.
3. Also measure the Voltages at Logic I/Ps for the UP & DOWN Position of the Switch.
4. Apply the Logic I/P 1 or 0 to A1 A0 control I/P
5. Apply the Logic I/P to D0 to D3 pins from the Logic I/Ps.
6. Connect the O/P Q to Logic O/P Indicator.
7. Note & Verify the Truth table for different combinations of control I/Ps.

Observation table:

I/P		O/P
A1	A0	Q
0	0	
0	1	
1	0	
1	1	

Using Bread Board-

1. Draw the circuit diagram and connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC.
5. Verify the truth table.

Result:

The 4:1 Multiplexer using IC 74153 is studied. The Multiplexer will produce the same Data at the O/P which is selected by the Control I/Ps.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

- Q.1 Explain the principle of Multiplexer?
- Q.2 Draw a circuit diagram of 4: 1 Multiplexer?
- Q.3 What are the advantages of Multiplexer?
- Q.4 What are the disadvantages of Multiplexer?
- Q.5 Make the Truth-table of Multiplexer?

EXPERIMENT NO.8

Objectives:

To Study 1:4 Demultiplexer Using Various IC's.

Appratus Required:

1. Trainer Kit Method: - Trainer Kit, Digital Multimeter, Patch Cords.
2. Bread Board Method:- Bread Board +5V DC Power Supply, LED and Hookup Wires, Digital Multimeter.

Components Required:

IC- 74139, IC-7408, IC-7404.

Theory:

Demultiplex means one into many. A Demultiplexer is a Logic Circuit with one I/P and many O/Ps. By Applying Control Signal, we can Steer the I/P Signal to one of the O/P lines.

Following fig shows the block Diagram of the Demultiplexer.

The Demultiplexer has 1 I/P Signal m Control Signals and n O/P Signals

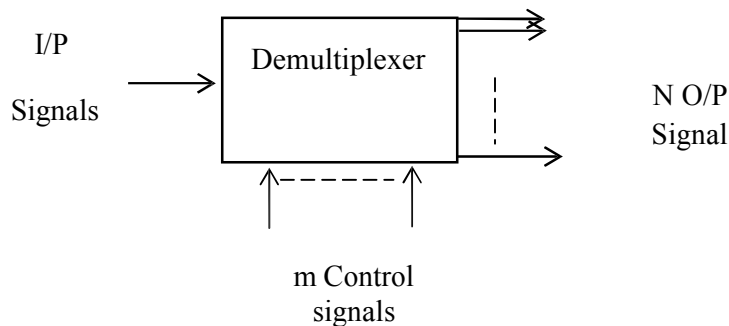


Fig :-1 Block Diagram of Demultiplexer

1 to 4 Demultiplexer:

The fig on the Front Panel of the Kit shows the 1:4 Demultiplexer using IC 74139. It has 1 I/P pin; 2 Control pins A1, A0 and 4 O/P pins Q0-Q3. Control Signal is applied to A1 A0 and O/P is taken from Q0 to Q3.

Depending upon the control Signal the Data at I/P is Produced at the respective O/P. For e.g. If the I/P to A1 A0 is 1 0 then the Data at I/P pin is produced at O/P Q2.

Following fig shows the Pin Configuration & Truth Table of IC 74139

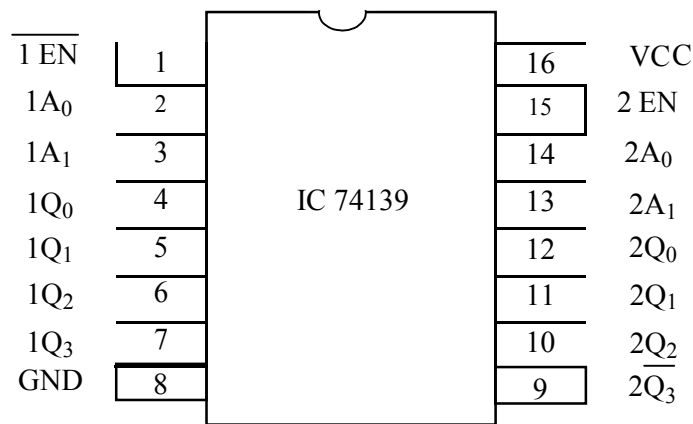


Fig 2: Pin out diagram of IC 74139

I/Ps			O/P
Enable	ADDR		Q = L
EN	A1	A0	
1	X	X	-
0	0	0	Q0
0	0	1	Q1
0	1	0	Q2
0	1	1	Q3

Procedure:

- (1) Study the circuit provided on the front panel of the circuit.
- (2) Switch ON the Power Supply.
- (3) Measure the Voltage at Pin no 16 using DMM.
- (4) Measure the Voltages at Logic I/Ps for the UP & DOWN Position of the Switch.
- (5) Apply the Logic I/P 1 or 0 to A1 A0 control select I/P & Enable Pin.
- (6) Keep Enable I/P at logic 0, vary the A1 A0 I/Ps & Verify the Truth table

Observation table:

I/P		O/P
A1	A0	Q
0	0	
0	1	
1	0	
1	1	

Using Bread Board-

1. Connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC.
5. Verify the truth table.

Result:

The 1:4 Demultiplexer using IC 74139 is studied. The Demultiplexer will Produce the Same Data from I/P to O/P Selected by the Control I/Ps.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

Q.1 Explain about Demultiplexer?

Q.2 Draw a circuit diagram of 1: 4 Demultiplexer?

Q.3 Make a logic diagram of 1: 4 Demultiplexer?

Q.4 What is the application of Demultiplexer?

Q.5 What is the difference between Multiplexer and Demultiplexer?

EXPERIMENT NO: 09

Objectives:

Design & implementation the Analog to Digital Converter using Op-Amp.

Apparatus Required:

Trainer Kit Method: - Trainer Kit, Patch cords

Bread Board Method: - Bread Board, +12V DC Power Supply, LED and Hookup Wires, Digital Multimeter.

Components Required:

IC 74148, IC741, Resistor = R1 to R7=10K.

Introduction:

Analog to Digital (A/D) conversion is a very important aspect of digital data processing. The process of changing an analog signal to an equivalent digital signal is accomplished by the use of an A/D converter. A/D converter is often referred to as an encoding device since it is used to encode signals for entry into a digital system.

Theory:

An analog to digital converter is a special type of encoder.

Following fig (1) shows the idea about A/D converter.

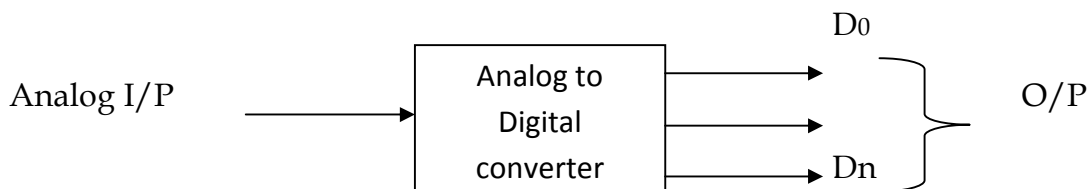


Fig (1)

Fig (2) shows the basic block diagram of A/D converter.

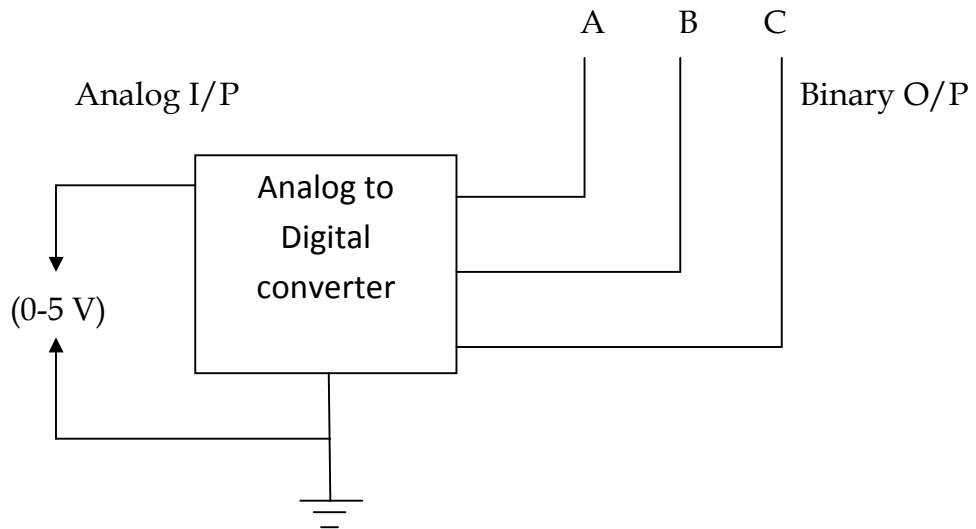
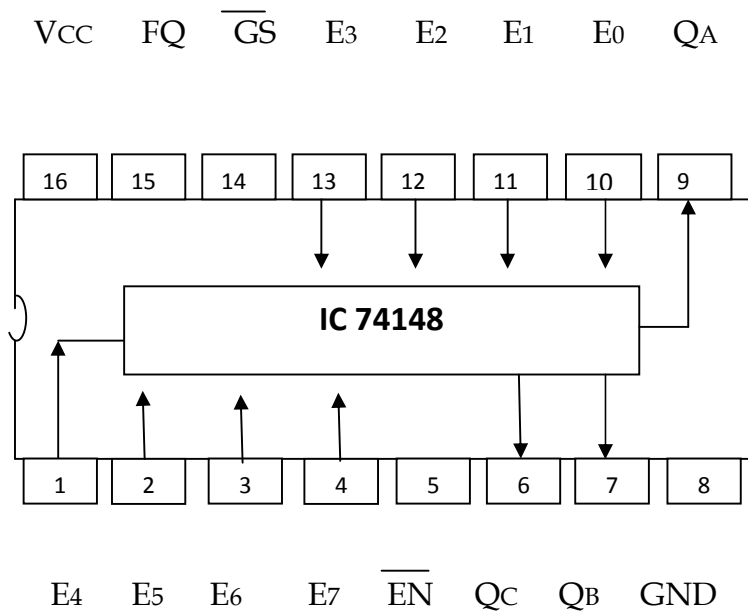


Fig (2)

The input is a variable voltage. The voltage in this case varies from 0 to 5 v. The output of the the A/D converter is in binary. The A/D converter translates the analog voltage at the input into a 3bit binary word.

IC 74148 (8 line to 3 line priority encoder) is shown in t



In priority encoder encoding matrix must accept seven input levels and encode them into 3-bit binary number having eight possible states.

Operation:

The simultaneous method of A/D conversion is based on the use of number of comparator circuits. The analog signal to be digitized serves as one of the I/P to each comparator. The second input is a standard reference voltage. The reference voltages are $1/8 V_R$, $1/4 V_R$, $3/8 V_R$, $1/2 V_R$, $5/8 V_R$, $3/4 V_R$ & $7/8 V_R$. If the analog input exceeds the reference voltage to any comparator that comparator turns ON. Now if all the comparators are OFF the analog input signal must be between 0 and $1/8 V_R$. If E7 is high (comparator 1 is ON) and other (2-----8) are low, the input must be between $1/8 V_R$ and $1/4 V_R$. If the O/P of comparator 1 and comparator 2 are high while comparator 3 is low then the input must be between $1/4 V_R$ and $3/8 V_R$. Finally if all comparator outputs are high the input signal must be between $7/8 V_R$ & $+V_R$.

Notice that in order to convert the input signal to a digital signal having 3 bits; it is necessary to have seven comparators. In general it can be said that 2^{n-1} comparator are required to convert to a digital signal that has n bits.

A convenient application for an IC 74148 priority encoder is to use it to replace all the digital logic. The inputs E1, E2-----E7 must be TTL-compatible. In essence, the output of the IC 74148 is a digital number that reflects the highest order zero input, this corresponds to the lowest reference voltage that still exceeds the input analog voltage. As the number of bits in the desired digital number increase, the numbers of comparators increase very rapidly. The Truth table is as follows.

Procedure:

1. Study the circuit diagram provided on the front panel of the kit.
2. Connect the analog I/P to Analog I/P of circuit by using patch chord.
3. Switch 'ON' the Power supply.
4. Change the Analog I/P voltage V_i in steps. Observe & note the corresponding O/ps Q_a , Q_b , Q_c and comparator level as per Truth Table.
5. Observe the Practical and Theoretical Value.

Observation Table:

$7/8 V_R$ =----- $3/4 V_R$ =----- $5/8 V_R$ = -----
 $1/2 V_R$ =----- $3/8 V_R$ =----- $1/4 V_R$ =-----
 $1/8 V_R$ =-----

Input Voltage	Binary Output		
	QC	QB	QA
0 - 0.5 V	0	0	0
0.5 - 1.25V	0	0	1
1.25 - 1.9V	0	1	0
1.9 - 2.5 V	0	1	1
2.5 - 3.0 V	1	0	0
3.0 - 3.76 V	1	0	1
3.76 - 4.38 V	1	1	0
4.38 - 5 V	1	1	1

Sr.No.	Theoretical I/P Volt	Comparator Level								Binary Output		
		E0	E1	E2	E3	E4	E5	E6	E7	QC	QB	QA

Using Bread Board-

1. Connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 4 is connecting the Ground or -12 V VCC. and Pin no. 7 connect the +12V VCC.
5. Verify the truth table.

Result:

By using OP-AMPS with Priority Encoders an Analog I/P can be converted into digital by simultaneous method of A/D converter.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

- Q.1 What is comparator?
- Q.2 How many types of Analog to Digital converter?
- Q.3 What is hazard?
- Q.4 What is successive approximation method of A to D converter?
- Q.5 Discuss the working of dual slope A to D converter with the help of logic diagram?

EXPERIMENT NO: 10

Objectives:

To study the Binary Weighted D to A Converter using IC-741.

Apparatus Required:

Trainer Kit Method: - Trainer Kit

Bread Board Method:- Bread Board, +12V DC Power Supply, LED and Hookup Wires, Digital Multimeter.

Components Required:

IC 741,

Resistor = 10K, 5K, 2.5K, 1.25K,

$R_F = 864\Omega$, $R_L = 10K$

Theory:

Digital to Analog conversion involves translation of digital information into equivalent analog information. Whereas Analog to Digital conversion involves the translation of analog information into equivalent digital information. Digital to Analog conversion is straight forward process and is considerably easier than A/D conversion. In fact, a D/A converter is usually an integral part of any A/D converter.

A D/A converter in its simplest form use an op-amp and either binary-weighted resistor or R & 2R resistors.

The circuit provided on the kit is of binary weighted resistor type. Although the op-amp is connected in inverting mode. Since the number of binary input is 4, the converter is called a 4-bit converter. Since there are 16 possible combinations of binary inputs (From B0 ----- B3), an analog output should have 16 possible corresponding values. The 4 switches (B0 to B3) are used to simulate the binary inputs. When switch B3 is at upward direction (i.e. +5V), the voltage across R is 5V because $V_2 = V_1 = 0V$. Due to this the current through R is $5V/10K = 0.5mA$. However, the input bias current I_B is negligible, hence the current through feedback resistor R_F is also 0.5mA, which in turn produces an output voltage of $-(1K)(0.5mA) = -0.5V$.

Now suppose that switch B2 is in high state and all others are at low state, cause twice current (1mA) to flow through RF, which in turn doubles the output voltage. Thus the output voltage V0 is -1V when B2 is at high state. Thus depending upon which switch are selected, the binary weighted current will be set up in input resistors. The sum of these currents is equal to the current through RF, which in turn is converted to a proportional output voltage. When all the switches are high, the output will be maximum. The output voltage equation is given by

Where inputs B3 ----- B0 may be either high (+5V) or low (0V).

$$V_0 = -R_F \left[\frac{B_3}{R} + \frac{B_2}{R/2} + \frac{B_1}{R/4} + \frac{B_0}{R/8} \right] \text{ ----- (1)}$$

Truth Table:

INPUTS				OUTPUTS
B3	B2	B1	B0	O/P
0	0	0	0	0
0	0	0	1	-0.5
0	0	1	0	-1.0
0	0	1	1	-1.5
0	1	0	0	-2.0
0	1	0	1	-2.5
0	1	1	0	-3.0
0	1	1	1	-3.5
1	0	0	0	-4.0
1	0	0	1	-4.5
1	0	1	0	-5.0
1	0	1	1	-5.5
1	1	0	0	-6.0
1	1	0	1	-6.5
1	1	1	0	-7.0
1	1	1	1	-7.5V

Procedure:

- 1) Study the circuit provided on the front panel of the kit.
- 2) Switch 'ON' the power supply.
- 3) Check the +12V and -12V at the pin no. 7 and pin no.4 of IC 741 respectively.
- 4) Apply the Input by selecting the switches from B0 ----- B3 to the I/P.
- 5) Observe the output on DMM.
- 6) Change the input B0 ----- B3 and observe the corresponding effect on DMM.
- 7) Compare this O/P with theoretical calculated from equation (1).

Observation Table:

INPUTS				OUTPUTS
B ₃	B ₂	B ₁	B ₀	O/P
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Using Bread Board-

1. Connect the circuit as per circuit diagram.
2. Connect the input terminal to the Input pins of IC.
3. Connect the Output terminal to the Logic Indicator.
4. Pin no. 4 is connecting the Ground or -12 V VCC. and Pin no. 7 connect the +12V VCC.
5. Verify the truth table.

Result:

Digital to Analog Converter is studied & analog voltage for different digital 4 bit input is also observed & Recorded in the Table Shown Below.

Draw the Circuit Diagram for Bread Board Method

VIVA QUESTIONS

- Q.1 Explain the working of D to A converter?
- Q.2 Explain the R -2R Ladder D to A converter?
- Q.3 Discuss the advantages of binary ladder network over a binary weighted resistor network in D to A converter?
- Q.4 Explain the working of weighted resistor network D to A converter?
- Q.5 Discuss the various the specification of D to A converter?
- Q.6 Name the other method for D to A convertor?

